Amendments of the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the above-identified patent application:

Listing of Claims

1. (currently amended) A serial interface for use in a programmable logic device, said serial interface comprising:

a plurality of channels, each of said channels including at least transmit circuitry;

central control circuitry including at least one clock source for generating at least one transmit clock for use by said transmit circuitry in each of said channels, each said transmit clock having a respective first clock rate; and

clock division circuitry in ~~at least one~~ a plurality of said channels for providing from at least one said transmit clock a channel-derived clock having a second clock rate at most equal to said respective first clock rate, said clock division circuitry in each of said plurality of channels being controllable independently of said clock division circuitry in any other of said plurality of channels.

2. (original) The serial interface of claim 1 wherein each of said channels includes said clock division circuitry.

3. (original) The serial interface of claim 1 wherein said clock division circuitry comprises a respective first divider that selectably divides said respective first clock rate by one of a group of at least one integer value.

4. (original) The serial interface of claim 3 wherein said one of said group of at least one integer value

is selected by user programming of said programmable logic device.

5. (original) The serial interface of claim 3 wherein said one of said group of at least one integer value is selected under control of logic in said programmable logic device.

6. (original) The serial interface of claim 3 wherein said group of at least one integer value consists of one integer value.

7. (original) The serial interface of claim 3 wherein said group of at least one integer value comprises a plurality of integer values.

8. (currently amended) The serial interface of claim 1 further comprising a selector for selecting as said channel-derived clock one of (a) one said at least one transmit clock, and (b) output of said clock division circuitry.

9. (original) The serial interface of claim 8 wherein said selector comprises a multiplexer.

10. (original) The serial interface of claim 1 wherein said at least one clock source consists of a single clock source generating a single transmit clock having a single transmit clock rate.

11. (original) The serial interface of claim 1 wherein said at least one clock source comprises a plurality of clock sources, each of said clock sources generating its own respective first clock rate.

12. (original) The serial interface of claim 11 further comprising a selector for selecting as said channel-derived clock one of (a) one of said plurality of clock sources, and (b) output of said clock division circuitry.

13. (original) The serial interface of claim 12 wherein said selector comprises a multiplexer.

14. (original) The serial interface of claim 11 wherein:

said clock division circuitry comprises a respective divider for dividing each said respective first clock rate by a respective selectable integer value; and

said serial interface further comprises a selector for selecting said channel-derived clock from among outputs of said respective dividers.

15. (original) The serial interface of claim 14 wherein said selector comprises a multiplexer.

16. (currently amended) [[The]] A serial interface ~~of claim 1 wherein~~ for use in a programmable logic device, said serial interface comprising:

a plurality of channels, each of said channels including at least transmit circuitry;

central control circuitry including:

at least one clock source for generating at least one transmit clock for use by said transmit circuitry in each of said channels, each said transmit clock [[is]] being a serial clock ~~and each said~~ having a respective first clock rate that is a serial clock rate[[;]], and

~~said central control circuitry further comprises,~~ for each said at least one clock source, a divider for deriving from each said transmit clock a respective parallel clock having a respective parallel clock rate; and

clock division circuitry in at least one of said channels for providing from at least one said transmit clock a channel-derived clock having a second clock rate at most equal to said respective first clock rate; wherein:

said clock division circuitry derives a channel-derived serial clock having a second clock rate at

most equal to said respective first clock rate, and a channel-derived parallel clock having a channel-derived parallel clock rate at most equal to said respective parallel clock rate.

17. (original) A programmable logic device comprising the serial interface of claim 1.

18. (original) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 17 coupled to the processing circuitry and the memory.

19. (original) A printed circuit board on which is mounted a programmable logic device as defined in claim 17.

20. (original) The printed circuit board defined in claim 19 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

21. (original) The printed circuit board defined in claim 20 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

22. (original) An integrated circuit device comprising the serial interface of claim 1.

23. (original) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

an integrated circuit device as defined in claim 22 coupled to the processing circuitry and the memory.

24. (original) A printed circuit board on which is mounted an integrated circuit device as defined in claim 22.

25. (original) The printed circuit board defined in claim 24 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

26. (original) The printed circuit board defined in claim 25 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

27. (currently amended) A programmable logic device comprising:

a programmable logic core; and

serial interface means comprising:

a plurality of channel means, each of said channel means including at least transmit means;

central control means including at least one clock means for generating at least one transmit clock for use by said transmit means in each of said channel means, each said transmit clock having a respective first clock rate; and

clock division means in ~~at least one~~ a plurality of said channel means for providing from at least one said transmit clock a channel-derived clock having a second clock rate at most equal to said respective first clock rate, said clock division means in each of said plurality of channels being controllable independently of said clock division means in any other of said plurality of channels.